PATENT ABSTRACTS OF JAPAN

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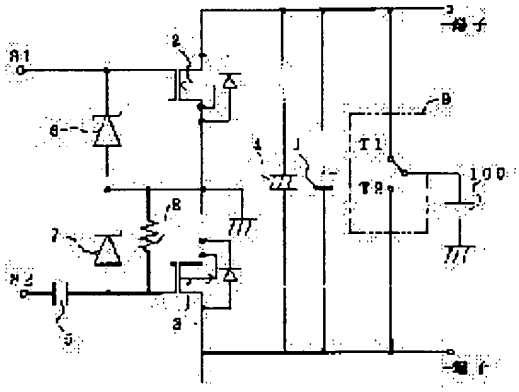
(54) LOAD DRIVING DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To output positive and negative AC voltages by using one power source without using two kinds of positive and negative power sources at the time of outputting the AC voltages to an EL element.

SOLUTION: A first FET 2 which makes and breaks the connection of the anode of the power source 1 and grounding voltage and a second FET 3 which makes and breaks the connection of the cathode of the power source 1 and the grounding voltage are alternately operated to turn on according to the control signal inputted to input terminals S1, S2 and further, the voltages of the anode and cathode of the power source 1 are selected by an output circuit 9 and are impressed on the EL element 100. Namely, the negative voltage is formed by the cathode of the power source 1 when the first FET 2 operates to turn on. The position voltage is formed from the anode of the power source 1 when the second FET 3 operates to turn on. These voltages are selectively outputted from the output circuit 9 and the AC voltage is impressed on the one electrode of the EL element 100.



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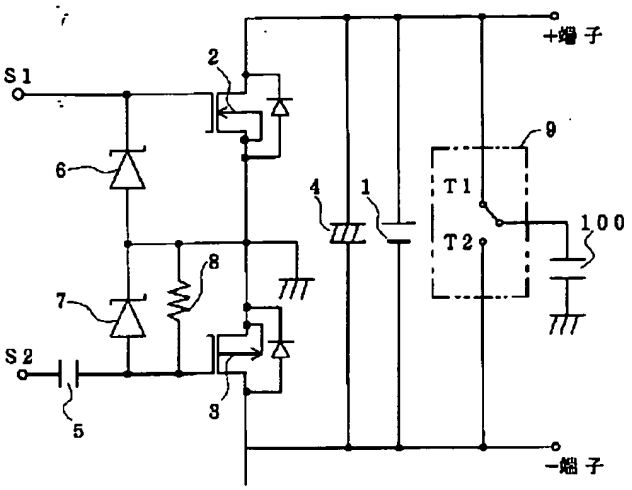
CLAIMS

[Claim(s)]
[Claim 1] The 1st switching means which opens and closes the anode plate of a power source (1) and this power source, and connection of the 1st reference voltage (2), It has the 2nd switching means (3) which opens and closes the cathode of said power source, and connection of the 2nd reference voltage. The said 1st and 2nd switching means is a load driving gear which carries out ON actuation alternatively according to a control signal, and is characterized by having a selection output means (9) to choose the electrical potential difference of the anode plate of said power source, and cathode further, and to output for the drive of a load.
[Claim 2] Said 1st and 2nd reference voltage is a load driving gear according to claim 1 characterized by being the same electrical potential difference.
[Claim 3] Said 1st and 2nd reference voltage is [both] a load driving gear according to claim 2 characterized by being a touch-down electrical potential difference.
[Claim 4] Said 1st and 2nd reference voltage is a load driving gear according to claim 1 characterized by being a mutually different electrical potential difference.
[Claim 5] Said selection output means is claim 1 characterized by being the drive circuit (20 30) which carries out the selection output of the electrical potential difference of the anode plate of said power source, and cathode, and performs a load drive in push pull actuation thru/or the load driving gear of any one publication of four.
[Claim 6] The said 1st and 2nd switching means is claim 1 characterized by being the transistor which has parasitism diode thru/or the load driving gear of any one publication of five.
[Claim 7] The 1st switching means which has the 1st power source (1) and 2nd power source (10), and opens and closes the anode plate of said 1st power source, and connection of reference voltage (2), It has the 2nd switching means (3) which opens and closes connection of the anode plate of said 2nd power source and the cathode of said 1st power source. The said 1st and 2nd switching means is what carries out ON actuation alternatively according to a control signal. The 1st drive circuit which furthermore chooses the electrical potential difference of the anode plate of said 1st power source, and cathode in push pull actuation, and outputs driver voltage to one electrode (201, 301 --) of an EL element (100) (20 30), It has the 2nd drive circuit (40) which outputs driver voltage to the electrode (401, 402 --) of another side of said EL element using the electrical potential difference of the anode plate of said 2nd power source. The driving gear of the EL element characterized by making it impress a polar driver voltage pulse which is different by FIRUDO of positive/negative to said EL element.

[Translation done.]

Drawing selection Representative drawing



[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the load driving gear which drives loads, such as EL (electroluminescence) component.
[0002]
[Description of the Prior Art] The typical cross-section configuration of an EL element is shown in drawing 7 . EL element 100 consists of the transparent electrode 102 and the 1st insulating layer 103 by which laminating formation was carried out, a luminous layer 104, the 2nd insulating layer 105, and a back plate 106 on the glass substrate 101, and alternating voltage is impressed between a transparent electrode 102 and a back plate 106, and it emits light.
[0003] Here, when a back plate 106 is grounded, if the alternating voltage of positive/negative is impressed to a transparent electrode 102, alternating voltage can be impressed to an EL element. Thus, when impressing the alternating voltage of positive/negative to one electrode, the power source of two kinds of positive/negative is needed, and there is usually a problem that a power circuit is enlarged. This invention is what took the example by the above-mentioned problem, and in case alternating voltage is outputted to loads, such as an EL element, it aims at impressing the alternating voltage of positive/negative to an EL element using one power source, without using the power source of two kinds of positive/negative.
[0004]
[Summary of the Invention] In order to attain the above-mentioned purpose, this invention carries out ON actuation of the anode plate of a power source, the 1st switching means which opens and closes connection of the 1st reference voltage, and the cathode of a power source and the 2nd switching means which opens and closes connection of the 2nd reference voltage alternatively according to a control signal, and is characterized [1st] by the point chooses the electrical potential difference of the anode plate of a power source, and cathode further, and it was made output for the drive of a load.
[0005] When the electrical potential difference by the side of the negative polarity [cathode / of a power source] on the basis of the 1st reference voltage when the 1st switching means carries out ON actuation by this is created and the 2nd switching means carries out ON actuation, the electrical potential difference by the side of the straight polarity on the basis of the 2nd reference voltage is created from the anode plate of a power source. Therefore, by choosing and outputting the created electrical potential difference, the alternating voltage of positive/negative is outputted with one power source, and loads, such as an EL element, can be driven with the output.
[0006] Moreover, although the 1st and 2nd switching means has the common thing of bidirection, in this invention, by using the transistor which has parasitism diode, it can use actuation of the parasitism DAIDO and can simplify a circuit. Moreover, the 1st switching means which this invention has the 1st power source and 2nd power source, and opens and closes the anode plate of the 1st power source, and connection of reference voltage, The 2nd switching means which opens and closes connection of the anode plate of the 2nd power source and the cathode of the 1st power source It is characterized [2nd] by the point make carry out ON actuation alternatively according to a control signal, and outputs driver voltage to one electrode of an EL element with the electrical potential difference of the anode plate of the 1st power source, and cathode further, and it was made to output driver voltage to the electrode of another side of an EL element using the electrical potential difference of the anode plate of the 2nd power source.
[0007] When the 1st switching means carries out ON actuation by this, reference voltage is outputted from the anode plate of the 1st power source, and the electrical potential difference by the side of the negative polarity on the basis of reference voltage is outputted from cathode. Moreover, when the 2nd switching means carries out ON actuation, the electrical potential difference by the side of the straight polarity which serves as the sum of each electrical potential difference of the 1st and 2nd power source from the anode plate of the 1st power source is outputted, and the electrical potential difference of the 2nd power source is outputted from cathode.

[0008] Therefore, the alternating voltage from which a polarity differs in the field of positive/negative can be impressed to an EL element, and an EL element can be made to emit light by being able to output four different electrical potential differences from the 1st power source, considering as the driver voltage of one electrode of an EL element with the output voltage, and considering as the driver voltage of the electrode of another side of an EL element by actuation of the 1st and 2nd switching means, using the electrical potential difference of the 2nd power source further. In that case, the 2nd power source can be used for creation of each driver voltage, and simplification of a circuit can be attained.
[0009]
[Embodiment of the Invention]
(The 1st operation gestalt) Drawing 1 is the circuit diagram showing the 1st operation gestalt of this invention. In the power circuit shown in this drawing 1 , it has the single power source 1 and that anode plate is grounded through the N channel (1st switching means) FET 2, and cathode is constituted so that it may be grounded through P channel FET (2nd switching means)3. Moreover, the capacitor 4 for smooth is formed in this power source 1 and juxtaposition.
[0010] A control signal is inputted into the N channel FET 2 from an input terminal S1, and a control signal is inputted into it through a coupling capacitor 5 at P channel FET3 from an input terminal S2. In addition, zener diodes 6 and 7 and resistance 8 are formed as an object for input protections. The output circuit 9 is established in the output stage of this power circuit, and that output voltage is impressed to one electrode of EL element 100. Moreover, the electrode of another side of EL element 100 is grounded.
[0011] In the above-mentioned configuration, it explains with reference to the timing chart which shows the actuation to drawing 2 . In addition, GND in drawing 2 shows the touch-down electrical potential difference. As shown in drawing 2 , the control signal of high level and a low level is inputted into input terminals S1 and S2. When both control signals are low level, the N channel FET 2 turns off and P channel FET3 turns on. Therefore, the electrical potential difference V of a power source 1 is outputted to + terminal, and a touch-down electrical potential difference is outputted to - terminal.
[0012] Moreover, when both control signals are high-level, the N channel FET 2 turns on and P channel FET3 turns off. Therefore, a touch-down electrical potential difference is outputted to + terminal, and the electrical potential difference of -V is outputted to - terminal. On the other hand, an output circuit 9 switches to the switch condition of T1 and T2 by turns to the timing which is interlocked with a control signal and shown in drawing 2 . The alternating voltage of drawing 2 by the electrical potential difference and touch-down electrical potential difference of V [**] is outputted with the switch. Since the alternating voltage is impressed to one side of EL element 100, EL element 100 emits light.
[0013] Since the N channel FET 2 turns on when S1 and S2 are high-level, if T1 turns on, an output will be set to GND at this time. Since P channel FET3 turns on if S1 and S2 are set to a low level, an output will be set to V if T1 remains as it is. If S1 and S2 remain as they are and T1 to T2 turns on, an output will be set to GND and the charge of an EL element will flow from T2 to GND through the parasitism diode of FET3. Time amount TP and TN to which an electrical potential difference is outputted by the switch timing of switches T1 and T2, and the change of state of S1 and S2 (pulse width) It is determined.
[0014] The concrete configuration of the output circuit 9 described above to drawing 3 is shown. The output circuit 9 has P channel FET9a and N channel FET9b, and according to the signal (signal interlocked with the control signal inputted into input terminals S1 and S2) of high level and a low level inputted from input terminals 9c and 9d, one of FET turns it on, and it is constituted so that one side of the electrical potential difference of + terminal and - terminal may be outputted. In addition, 9e and 9f in drawing are parasitism diodes.
[0015] In the above-mentioned operation gestalt, although what outputs the alternating voltage of V [**] on the basis of a touch-down electrical potential difference was shown, the 2nd power source which generates not a touch-down electrical potential difference but predetermined reference voltage for the electrical potential difference connected to a power source 1 through FET 2 and 3, then the alternating voltage centering on the reference voltage can be outputted. In this case, if the same electrical potential difference as reference voltage to describe above to the electrode of another side of an EL element is impressed, EL element 100 can be made to emit light like the above-mentioned operation gestalt.
(The 2nd operation gestalt) In the above-mentioned 1st operation gestalt, although the circuit which makes an EL element only emit light was shown, an EL element can also perform a segment display or a matrix display. In this operation gestalt, what performs a matrix display by the EL element is explained.
[0016] The whole EL display configuration which shows this 2nd operation gestalt to drawing 4 is shown. EL display-panel 100' in this EL display arranges on a matrix two or more transparent electrodes 102 of an EL element shown in drawing 7 , and back plates 106, and is constituted as a scan electrode and a data electrode. Drawing 4 is the odd number scan electrodes 201 and 202, --, an example by which the even number scan electrodes 301 and 302 and -- are

formed, and the data electrodes 401, 402, and 403 and -- are formed in the direction of a train at a line writing direction.

[0017] EL elements 111 and 112 as a pixel, --121, and -- are formed in the data electrodes 401, 402, and 403 and each crossover field with -- with the scan electrodes 201, 301, 202, and 302 and --. In addition, since an EL element is a capacitive component, it is expressed with the notation of a capacitor by a diagram. In order to perform the display drive of this EL display-panel 100', the scan side driver ICs 20 and 30 and the data side driver IC 40 are formed.
[0018] The scan side driver IC 20 is a push pull type drive circuit, has the N channels 21b and FET 22b and -- with the odd number scan electrodes 201 and 202, P channel FET 21a and 22a connected to --, and --, and impresses a scan electrical potential difference to the odd number scan electrodes 201 and 202 and -- according to the output from a control circuit 200. Moreover, the parasitism diodes 21c, 21d, 22c, and 22d and -- are formed in FET 21a, 21b, 22a, and 22b and each of --, and the electrical potential difference of a scan electrode is set as desired reference voltage.
[0019] With the same configuration, the scan side driver IC 30 also has the N channels 31b and FET 32b and -- with 300 or P control circuits 31a and FET 32a and --, and supplies a scan electrical potential difference to the even number scan electrodes 301 and 302 and --. Similarly, the data side driver IC 40 also has the N channels 41b and FET 42b and -- with 400 or P control circuits 41a and FET 42a and --, and supplies a data electrical potential difference to the data electrodes 401, 402, and 403 and --.
[0020] The configuration of the electrical-potential-difference supply circuit A which performs electrical-potential-difference supply to the scan side driver ICs 20 and 30 described above to drawing 5 and the data side driver IC 40 is shown. In drawing 5 , the 2nd power source 10 which outputs an electrical potential difference Vm is formed in the electrical-potential-difference supply circuit A, that cathode and anode plate of the 2nd power source 10 are connected, and a power source 1 (henceforth the 1st power source in this 2nd operation gestalt) outputs the electrical potential difference on the basis of an electrical potential difference Vm from the anode plate of the 1st power source, when P channel FET3 turns on.
[0021] The 2nd power source 10 supplies an electrical potential difference Vm and a touch-down electrical potential difference to the data side driver IC 40 through the electrical-potential-difference supply lines L3 and L4. Moreover, the 1st power source 1 supplies the electrical potential difference for forming a scan electrical potential difference through the electrical-potential-difference supply lines L1 and L2 to the scan side driver IC 3. In addition, the 1st power source 1 shall have the electrical potential difference of Vr-Vm in this operation gestalt. Here, Vr shows driver voltage required for luminescence.
[0022] Moreover, the configuration the same as that of what a control signal is inputted through filter circuits 11 and 12, and is shown in drawing 1 with other configurations, and the thing shown in drawing 1 about the part by which the same sign was attached, or equal is shown in the N channel FET 2 and P channel FET3. Although sufficient electrical potential difference for luminescence is required for the power source 1 of drawing 1 , the power source 1 of drawing 5 has the need below a luminescence threshold.
[0023] In the above-mentioned configuration, like what is shown in drawing 1 , if the control signal of a low level is inputted into input terminals S1 and S2, the N channel FET 2 turns off and P channel FET3 turns on. Therefore, the electrical potential difference Vm of the 2nd power source 10 is outputted to the electrical-potential-difference supply line L2 from the cathode of the 1st power source 1, and an electrical potential difference Vr (= Vr-Vm+Vm) is outputted to the electrical-potential-difference supply line L1 from an anode plate.
[0024] Moreover, if a high-level control signal is inputted into input terminals S1 and S2, the N channel FET 2 turns on and P channel FET3 turns off. Therefore, the electrical potential difference of -Vr+Vm is outputted to the electrical-potential-difference supply line L2 from the cathode of the 1st power source 1, and a touch-down electrical potential difference is outputted to the electrical-potential-difference supply line L1 from an anode plate. Therefore, in the drive of the forward field mentioned later, when it is the drive of the negative field which the electrical potential difference of Vr and Vm is outputted from the electrical-potential-difference supply lines L1 and L2, respectively, and is mentioned later (when both the control signals to input terminals S1 and S2 are low level), a touch-down electrical potential difference and the electrical potential difference of -Vr+Vm are outputted from the electrical-potential-difference supply lines L1 and L2, respectively (when both the control signals to input terminals S1 and S2 are high-level).
[0025] In the above-mentioned configuration, an EL element is explained with reference to the timing chart of drawing 6 about the actuation in the case of carrying out a matrix drive in the field of positive/negative.
(Forward field) Both the control signals to the input terminals S1 and S2 of drawing 5 are made into a low level. As described above by this, the electrical potential difference of Vr and Vm is outputted from the electrical-potential-difference supply lines L1 and L2, respectively. Moreover, the electrical potential difference and touch-down electrical potential difference of Vm are outputted from the electrical-potential-difference supply lines L3 and L4, respectively.
[0026] At this time, the scan electrodes 201, 301, 202, and 302 and the electrical potential difference of -- are an electrical potential difference Vm by actuation of the parasitism diode of FET of the scan side driver ICs 20 and 30.

Moreover, FET [of the data side driver IC 40]a [41],a [42], and 43a and -- side is turned on, and the electrical potential difference of a data electrode is set to Vm. In this condition, since the electrical potential difference impressed to all EL elements is set to 0V, an EL element does not emit light.
[0027] Then, luminescence actuation in the forward field is started. First, P channel FET21a of the scan side driver IC 20 connected to the scan electrode 201 of the 1st line is turned ON, and the electrical potential difference of the scan electrode 201 is set to Vr. Moreover, the output stage FET of the scan side driver ICs 20 and 30 connected to other scan electrodes is turned OFF altogether, and those scan electrodes are made into floating.
[0028] Moreover, ON and the N channel FET are turned OFF for P channel FET of the data side driver IC 40 connected [channel / FET / OFF and / N] to the data electrode of an EL element [an EL element / turns ON and] to make it emit light in P channel FET of the data side driver IC 40 connected to the data electrodes 401, 402, and 403 and the data electrode of an EL element [an EL element / --] to make it emit light inside.
[0029] By this, since the electrical potential difference of the data electrode of an EL element [an EL element] to make it emitting light turns into a touch-down electrical potential difference, the electrical potential difference Vr more than a threshold electrical potential difference is built over an EL element, and an EL element emits light. Moreover, the electrical potential difference of the data electrode of an EL element [an EL element] to make it emitting light serves as as [Vm], and the electrical potential difference of Vr-Vm is impressed to an EL element. The electrical potential difference of this Vr-Vm is set up lower than a threshold electrical potential difference, and an EL element does not emit light.
[0030] By the timing chart of drawing 6 , OFF and N channel FET41b are turned ON for P channel FET41a of the data side driver IC 40, the electrical potential difference of Vr is impressed to EL element 111, and the condition of making EL element 111 emitting light is shown. Then, the charge accumulated in the EL element on the scan electrode 201 is discharged by turning OFF P channel FET21a of the scan side driver IC 20 connected to the scan electrode 201 of the 1st line, and turning on N channel FET21b.
[0031] Next, P channel FET31a of the scan side driver IC 3 connected to the scan electrode 301 of the 2nd line is turned on, and the electrical potential difference of the scan electrode 301 is set to Vr. Moreover, the output stage FET of the scan side driver ICs 20 and 30 connected to other scan electrodes is turned OFF altogether, and those scan electrodes are made into floating. Moreover, the luminescence drive of an EL element of the 2nd line is performed the same with having described above by considering as the data electrodes 401, 402, and 403 and the voltage level according to the EL element [an EL element / a voltage level] of -- making it emit light, and an EL element [an EL element] making it emit light.
[0032] By the timing chart of drawing 6 , ON and N channel FET41b are turned OFF for P channel FET41a of the data side driver IC 40, the electrical potential difference of Vr-Vm is impressed to EL element 121 by setting the electrical potential difference of the data electrode 401 to Vm, and the condition of not making EL element 121 emitting light is shown. Then, the charge accumulated in the EL element on the scan electrode 301 is discharged by turning OFF P channel FET31a of the scan side driver IC 3 connected to the scan electrode 301 of the 2nd line, and turning on N channel FET31b.
[0033] Henceforth, similarly, line sequential scanning which repeats the above-mentioned actuation is performed until it results in the last scanning line.
(Negative field) The control signal to the input terminals S1 and S2 of drawing 5 is both made high-level. As described above by this, a touch-down electrical potential difference and the electrical potential difference of -Vr+Vm are outputted from the electrical-potential-difference supply lines L1 and L2, respectively.
[0034] At this time, a scan electrode serves as a touch-down electrical potential difference by actuation of the parasitism diode of the scan driver ICs 20 and 30. Moreover, FET 41b, 42b, and 43b of the data side driver IC 40 -- A side is turned on and the electrical potential difference of a data electrode is made into a touch-down electrical potential difference. In this condition, since the electrical potential difference impressed to all EL elements is set to 0V, an EL element does not emit light. Hereafter, line sequential scanning is performed like [the negative field] the forward field.

[0035] -Vr+Vm is impressed to the scan electrode of the line which performs display selection. Contrary to the forward field, the electrical potential difference of a data electrode [an electrode] to make it emitting light is left a touch-down electrical potential difference at a data electrode side to a data electrode [want / Vm / he / to emit light by carrying out]. To therefore, the EL element to it if an electrical potential difference Vm is impressed to a data electrode to the scan electrode with which the electrical potential difference of -Vr+Vm is impressed - The electrical potential difference of Vr is impressed and an EL element emits light. Moreover, since -Vr+Vm lower than a threshold electrical potential difference is impressed to an EL element as the electrical potential difference of a data electrode is a touch-down electrical potential difference, an EL element does not emit light.
[0036] And the display action of 1 cycle is completed by the drive of the above-mentioned positive/negative field, and

it carries out by repeating this. In this 2nd operation gestalt, the electrical potential difference Vm used for the drive at the time of the forward field functions as offset voltage. That is, in the forward field, the electrical potential difference of Vr-Vm is impressed to the scan side driver ICs 20 and 30, and the electrical potential difference of -Vr+Vm is impressed to them in the negative field. Therefore, pressure-proofing of the scan side driver ICs 20 and 30 can be made low by offset voltage Vm, and low pressure-proofing-ization of the scan side driver ICs 20 and 30 can be attained.
[0037] Moreover, since it is made to change from offset voltage Vm to the electrical potential difference Vr for a drive at the time of luminescence timing, the electrical-potential-difference change can be made small, the peak current which flows to an EL element can be made low, and the dependability of an EL element can be raised. As an operation gestalt in a segment display, a data side driver IC is lost in drawing 5 , and one side of the electrode of an EL element is set to GND. And a power source 10 is also abolished and the source of FET3 is set to GND. In this case, the current supply circuit A is equivalent to drawing 1 . In addition, in order to make EL emit light at this time, a power source 1 needs to be sufficient electrical potential difference for luminescence.
[0038] In addition, although what applies this invention to the drive circuit of an EL element was shown, if the load which operates in response to the alternating voltage of positive/negative from one output line is driven, this invention is applicable in the above-mentioned various operation gestalten, besides an EL element. In that case, in what is shown in the 1st operation gestalt, the electrical potential difference of the positive/negative created is alternatively outputted in push pull actuation, and it may be made to carry out a load drive.
[0039] Moreover, although a driver IC is the push pull of the structure which connected the N channel FET with P channel FET, the push pull driver which consisted of N channels FET is sufficient. Moreover, the bipolar transistor of NPN and PNP may be used instead of 2 or P N channel FET FET3, respectively.

[Translation done.]

* NOTICES * ·

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[Field of the Invention] This invention relates to the load driving gear which drives loads, such as EL (electroluminescence) component.

[Translation done.]

TECHNICAL PROBLEM

[Description of the Prior Art] The typical cross-section configuration of an EL element is shown in drawing 7 . EL element 100 consists of the transparent electrode 102 and the 1st insulating layer 103 by which laminating formation was carried out, a luminous layer 104, the 2nd insulating layer 105, and a back plate 106 on the glass substrate 101, and alternating voltage is impressed between a transparent electrode 102 and a back plate 106, and it emits light.
[0003] Here, when a back plate 106 is grounded, if the alternating voltage of positive/negative is impressed to a transparent electrode 102, alternating voltage can be impressed to an EL element. Thus, when impressing the alternating voltage of positive/negative to one electrode, the power source of two kinds of positive/negative is needed, and there is usually a problem that a power circuit is enlarged. This invention is what took the example by the above-mentioned problem, and in case alternating voltage is outputted to loads, such as an EL element, it aims at impressing the alternating voltage of positive/negative to an EL element using one power source, without using the power source of two kinds of positive/negative.
[0004]
[Summary of the Invention] In order to attain the above-mentioned purpose, this invention carries out ON actuation of the anode plate of a power source, the 1st switching means which opens and closes connection of the 1st reference voltage, and the cathode of a power source and the 2nd switching means which opens and closes connection of the 2nd reference voltage alternatively according to a control signal, and is characterized [1st] by the point chooses the electrical potential difference of the anode plate of a power source, and cathode further, and it was made output for the drive of a load.
[0005] When the electrical potential difference by the side of the negative polarity [cathode / of a power source] on the basis of the 1st reference voltage when the 1st switching means carries out ON actuation by this is created and the 2nd switching means carries out ON actuation, the electrical potential difference by the side of the straight polarity on the basis of the 2nd reference voltage is created from the anode plate of a power source. Therefore, by choosing and outputting the created electrical potential difference, the alternating voltage of positive/negative is outputted with one power source, and loads, such as an EL element, can be driven with the output.
[0006] Moreover, although the 1st and 2nd switching means has the common thing of bidirection, in this invention, by using the transistor which has parasitism diode, it can use actuation of the parasitism DAIDO and can simplify a circuit. Moreover, the 1st switching means which this invention has the 1st power source and 2nd power source, and opens and closes the anode plate of the 1st power source, and connection of reference voltage, The 2nd switching means which opens and closes connection of the anode plate of the 2nd power source and the cathode of the 1st power source It is characterized [2nd] by the point make carry out ON actuation alternatively according to a control signal, and outputs driver voltage to one electrode of an EL element with the electrical potential difference of the anode plate of the 1st power source, and cathode further, and it was made to output driver voltage to the electrode of another side of an EL element using the electrical potential difference of the anode plate of the 2nd power source.
[0007] When the 1st switching means carries out ON actuation by this, reference voltage is outputted from the anode plate of the 1st power source, and the electrical potential difference by the side of the negative polarity on the basis of reference voltage is outputted from cathode. Moreover, when the 2nd switching means carries out ON actuation, the electrical potential difference by the side of the straight polarity which serves as the sum of each electrical potential difference of the 1st and 2nd power source from the anode plate of the 1st power source is outputted, and the electrical potential difference of the 2nd power source is outputted from cathode.
[0008] Therefore, the alternating voltage from which a polarity differs in the field of positive/negative can be impressed to an EL element, and an EL element can be made to emit light by being able to output four different electrical potential differences from the 1st power source, considering as the driver voltage of one electrode of an EL element with the output voltage, and considering as the driver voltage of the electrode of another side of an EL element by actuation of the 1st and 2nd switching means, using the electrical potential difference of the 2nd power source further.

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In that case, the 2nd power source can be used for creation of each driver voltage, and simplification of a circuit can be attained.

[0009]

[Embodiment of the Invention]

(The 1st operation gestalt) Drawing 1 is the circuit diagram showing the 1st operation gestalt of this invention. Having the single power source 1 in the power circuit shown in this drawing 1 , that anode plate is the N channel FET.

[Translation done.]

MEANS

(1st switching means) It is grounded through 2 and cathode is P channel FET.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram showing the 1st operation gestalt of this invention.
[Drawing 2] It is the timing chart which shows actuation of each part in drawing 1 .
[Drawing 3] It is the circuit diagram showing the concrete configuration of the output circuit in drawing 1 .
[Drawing 4] It is the whole EL display block diagram showing the 2nd operation gestalt of this invention.
[Drawing 5] It is the block diagram showing the configuration of the electrical-potential-difference supply circuit concerning the 2nd operation gestalt of this invention.
[Drawing 6] It is a drive timing chart in the configuration of drawing 4 .
[Drawing 7] It is the typical cross-section block diagram of an EL element.
[Description of Notations]
1 10 [-- A scan side driver IC, 40 / -- A data side driver IC, 100 / -- An EL element, 100' / -- EL display panel.] -- A power source, 2 -- The N channel FET, 3--P channel FET, 9 -- 20 An output circuit, 30

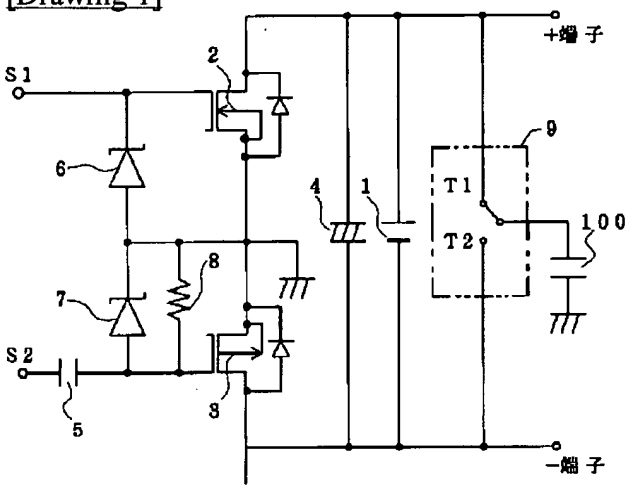
[Translation done.]

* NOTICES * ・

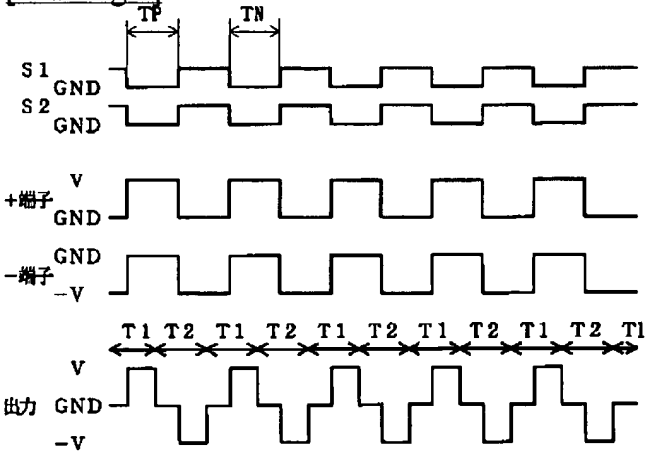
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

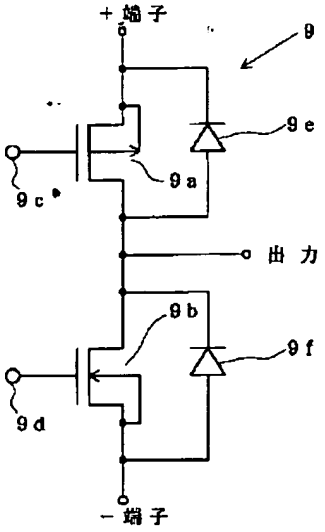
[Drawing 1]



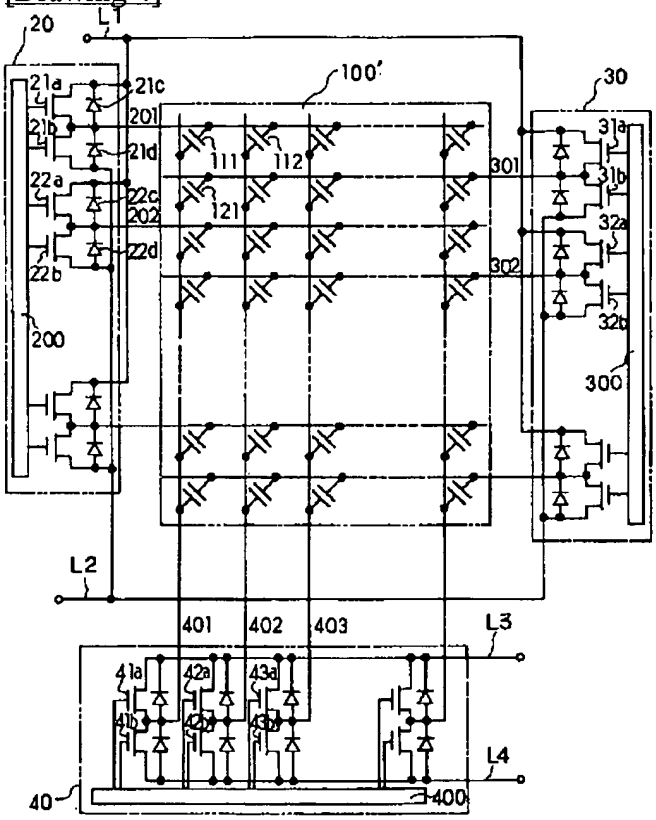
[Drawing 2]



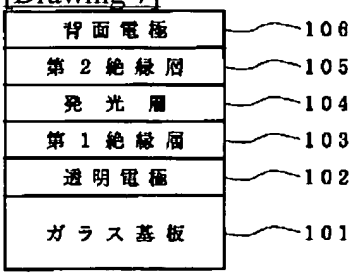
[Drawing 3]



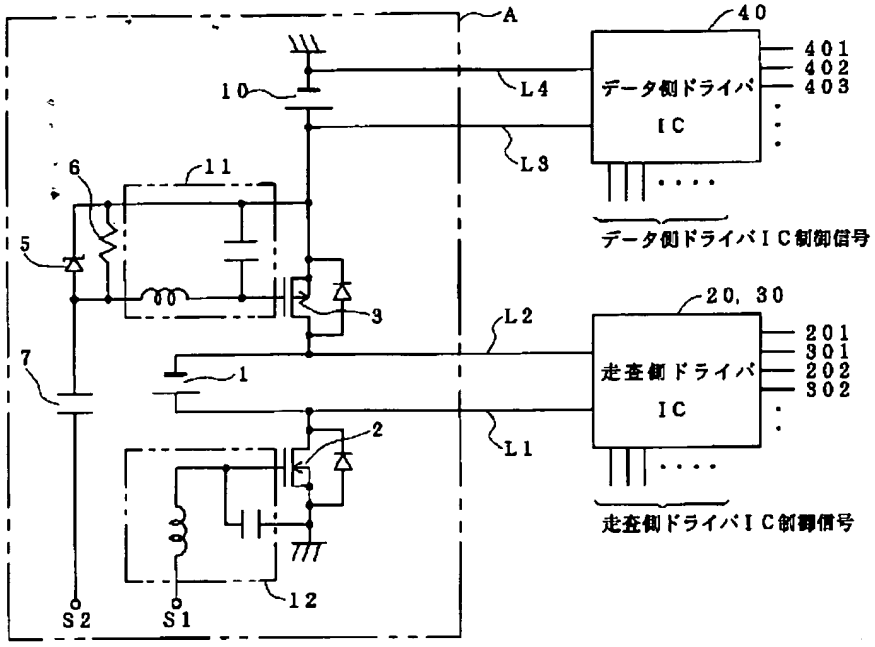
[Drawing 4]



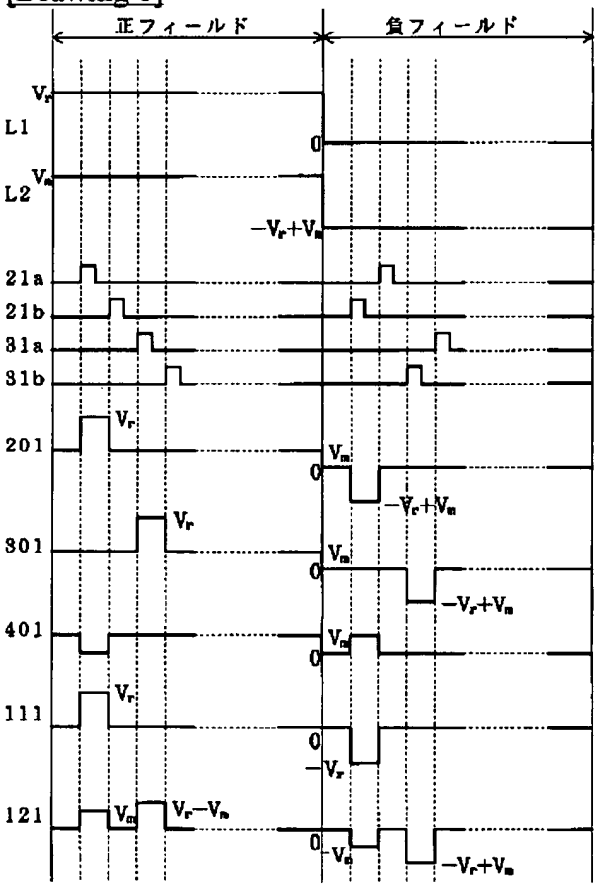
[Drawing 7]



[Drawing 5]



[Drawing 6]



[Translation done.]